

Claim Rejections - 35 USC §102

The Examiner also rejects Claims 52-54, 57-59, 61-69 and 71 under 35 USC §102(e) as being anticipated by Kimura et al. (US 6,157,429)¹. This rejection is respectfully traversed.

More specifically, in the Office Action, the Examiner is contending that Kimura '962 discloses a semiconductor substrate 1 at col. 37, ln. 11 in the reference. Applicants respectfully disagree.

Kimura '962 at col. 37, ln. 11 states “the PIN diode 110 is formed on the TFT array substrate 1 using the same semiconductor film used for the formation of the switching TFT 221 and the current TFT 223, and PIN junction formed by impurity doping.” What this sentence is clearly stating is that the PIN diode 110 is formed using the same semiconductor film as is used for the switching TFT 221, etc. This sentence does not state that the substrate is formed using the same semiconductor film (which appears to be the basis for the Examiner’s rejection) as the switching TFT 221. Applicants’ interpretation is supported by the context of the statement and the patent and the counterpart publication in Japan (WO98/40871).

Hence, Kimura '962 does not disclose or suggest a semiconductor substrate, and therefore, cannot anticipate the claims of the present application.

Claim Rejections - 35 USC §103

The Examiner also has the following rejections under 35 USC §103(a):

¹ The citation to US 6,157,429 in the Office Action is believed to be in error. It is believed that the Examiner is referring to US 6,518,962 (Kimura et al.; hereinafter Kimura '962) which is listed on the PTO 892 form attached to the Office Action. This is the reference Applicants are responding to in this Response. If the Examiner’s rejection is based on another reference, then this Office Action should be reissued and, reference the proper reference.

- A. Claims 42-45, 47-49 and 51 are rejected as being unpatentable over Kimura et al. ('962) in view of Shields (US 4,839,707).
- B. Claims 46 and 50 are rejected as being unpatentable over Kimura et al. ('962) and Shields and further in view of Ue et al. (US 5,733,661).
- C. Claims 55, 60, 65 and 71 are rejected as being unpatentable over Kimura et al. ('962) in view of Ue et al.

Independent Claims 42, 47 and 51 each are directed to a display device having a semiconductor substrate. Claims 42 and 47 further recite an insulating layer formed on the semiconductor substrate.

As explained above, Kimura '962 does not disclose a semiconductor substrate. Further, there is no motivation or suggestion to use a semiconductor substrate in Kimura '962, and therefore, no motivation or suggestion to combine Kimura '962 with the alleged insulating layer in Shields. Therefore, independent Claims 42, 47 and 51 and the rejected dependent claims are not disclosed or suggested by the cited references and are patentable thereover.

Accordingly, it is respectfully requested that this rejection be withdrawn.

Information Disclosure Statement

Applicants are also filing an information disclosure statement (IDS) herewith. It is respectfully requested that this IDS be entered and considered by the Examiner prior to the issuance of a further action on this application.

Conclusion

It is respectfully submitted that the present application is in a condition for allowance and should be allowed.

If any fee is due for this response, please charge our deposition account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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